AMENDMENTS

In the Drawings

Figure 4 has been amended to include a reference number 400.

In the Specification

Please replace paragraph on page 16, lines 1 - 12 with the following paragraph:

There are several exceptions that may be raised with this instruction when an invalid or erroneous operation is attempted. In one embodiment, a first exception that may be raised is the TLB refill exception which indicates that a virtual address referenced by the LDV instruction does not match any of the TLB entries. Another exception is the TLB invalid exception that indicates when the referenced virtual address matches an invalid TLB entry. A third exception that may be raised is the Bus Error exception that indicates when a bus error is requested by the external logic, such as included in memory controller **222**, to indicate events such as bus time out, invalid memory address, or invalid memory access type. A fourth exception is the Address Error exception which indicates that the referenced virtual address is not aligned to a proper boundary.

Please replace the paragraph on page 28, lines 12 - 23 with the following paragraph:

In Application programs **132** that handle large amounts of vector data, such as multimedia processing, large blocks of vector data comprise a major portion of the data used by the programs. Performance of D-cache **204** is greatly enhanced with the present invention since VTU 138 offloads D-cache **204** from handling large blocks of vector data. Using VTU **138**, each vector can reside in any page and the cost of switching page boundaries is amortized over the entire transaction by using long burst transfers. At the application level, the compiler can extract vector streams and exercise an efficient scheduling mechanism to achieve performance improvements. Additionally, scatter/gather operations can be implemented in the present invention by allowing both read and write-back bursts which stride through memory **210**. In contrast, D-cache **204** line fill mechanisms can only implement unit stride transfers efficiently.

Please replace the paragraph on page 25, lines 12 - 16 with the following paragraph:

If kernel **506** alternatively performs context switch **522**, second application program **504** resumes execution until finished. Before performing context switch **528**, second application program **504** issues SyncVT and FVB instructions, and bit VBI is cleared, as shown in block **530**. Since bit VBI is cleared, bit VBL will be cleared during context switch **524** to first application program **502**.